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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/618,405	07/18/2000	Khaim Yong Tan	70990061-1	9784

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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/618,405	TAN ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-9 and 11-16* is/are allowed.

6)☒ Claim(s) *2 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 1/5/2004. Claims 2-16 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Kuddes (USP 5,638,410), newly cited prior art. Figure 1 of Kuddes shows a clock synchronization circuit for generating an output clock signal (CLK OUT) that is substantially in synchronization with a reference clock signal (ϕ1) when in synchronization state with a phase difference between the two clock signals of less than a predetermined value, the clock synchronization circuit comprising a programmable delay line (132) coupled to the reference clock signal (ϕ1), via DDL 112 and SW 114, to produce a delay adjusted delayed output clock signal that becomes increasingly closer to being in synchronization with the reference clock signal, and a phase detector (124) coupled to the reference clock signal for detecting a phase difference between the two clock signals and for generating an in synchronization signal (126) when the in-synchronization state is reached, wherein the in synchronization signal is a pulse having a pulse width sufficient to interrupt a microprocessor (130) as called for in claim 1.

2. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Hamilton et al. (USP 5,646,519), newly cited prior art. Figure 6 of Hamilton et al. shows a clock synchronization circuit for generating an output clock signal (output of 17) that is substantially in synchronization

with a reference clock signal (C1) when in synchronization state with a phase difference between the two clock signals of less than a predetermined value, the clock synchronization circuit comprising a programmable delay line (2) coupled to the reference clock signal (C1) to produce a delay adjusted delayed output clock signal that becomes increasingly closer to being in synchronization with the reference clock signal, and a phase detector (3) coupled to the reference clock signal for detecting a phase difference between the two clock signals and for generating an in synchronization signal (B) when the in-synchronization state is reached, wherein the in synchronization signal is a pulse having a pulse width sufficient to interrupt a microprocessor (μP) as called for in claim 1.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuddes (USP 5,638,410). Figure 1 of Kuddes shows a clock synchronization circuit for generating an output clock signal (CLK OUT) that is substantially in synchronization with a reference clock signal (ϕ1) when in synchronization state with a phase difference between the two clock signals of less than a predetermined value, the clock synchronization circuit comprising a programmable delay line (132) coupled to the reference clock signal (ϕ1), via DDL 112 and SW 114, to produce a delay adjusted delayed output clock signal that becomes increasingly closer to being in synchronization with the reference clock signal, and a phase detector (124) coupled to the

reference clock signal for detecting a phase difference between the two clock signals and for generating an in synchronization signal (126) when the in-synchronization state is reached, wherein the in synchronization signal is a pulse having a pulse width sufficient to interrupt a microprocessor (130). Kuddes does not disclose the clock synchronization circuit is implemented in a programmable gate array as called for in claim 10. However, it is notoriously well known that the programmable gate array is easy to implement at a low cost. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to implement Kuddes' clock synchronization circuit in a programmable gate array because it is cheap and easy to implement.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamilton et al. (USP 5,646,519). . Figure 6 of Hamilton et al. shows a clock synchronization circuit for generating an output clock signal (output of 17) that is substantially in synchronization with a reference clock signal (C1) when in synchronization state with a phase difference between the two clock signals of less than a predetermined value, the clock synchronization circuit comprising a programmable delay line (2) coupled to the reference clock signal (C1) to produce a delay adjusted delayed output clock signal that becomes increasingly closer to being in synchronization with the reference clock signal, and a phase detector (3) coupled to the reference clock signal for detecting a phase difference between the two clock signals and for generating an in synchronization signal (B) when the in-synchronization state is reached, wherein the in synchronization signal is a pulse having a pulse width sufficient to interrupt a microprocessor (μP). Hamilton et al. does not disclose the clock synchronization circuit is implemented in a programmable gate array as called for in claim 10. However, it is notoriously well known that

the programmable gate array is easy to implement at a low cost. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to implement Hamilton's clock synchronization circuit in a programmable gate array because it is cheap and easy to implement.

Allowable Subject Matter

Claims 3-9 and 11-16 are presently allowed.

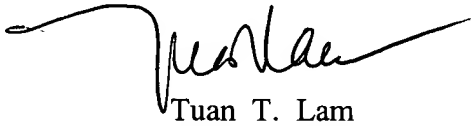
Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan T. Lam
Primary Examiner
Art Unit 2816

3/9/2004